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EXAMINER	
WASSUM, LUKE S	

ART UNIT	PAPER NUMBER
2177	9

DATE MAILED: 10/29/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/643,316	BROOKLER ET AL.	
	Examiner	Art Unit	
	Luke S. Wassum	2177	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 July 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-63* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-63* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *21 August 2000* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☒ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after a non-final rejection. Since prosecution has not been closed in this application, however, it is ineligible for continued examination under 37 CFR 1.114.

2. Accordingly, a Notice of Improper Request for Continued Examination was mailed on 1 October 2003. The amendment and arguments are being considered as a normal response to a non-final rejection, and an Office action based on said amendment and arguments follows.

Priority

3. The Applicants' claim to domestic priority under 35 U.S.C. §119(e) to provisional patent application 60/149,855, filed 19 August 1999, is acknowledged.

Drawings

4. In the Remarks section of the Applicants' response to the previous Office action, the Applicants state that they have submitted a hand-corrected copy of Figure 3 in response to the examiner's drawing objections. However, the proposed drawing amendment was not included with the Applicants' submission.

5. Since the Applicants' failure to respond to the drawing objection was apparently inadvertent, the application will not be abandoned. However, the Applicants are reminded that a proposed

drawing correction or corrected drawings are required in reply to this Office action **in order to avoid abandonment of the application.**

6. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(4) because reference characters "320-322" have been used to designate records in both the manufacturers and categories tables. A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

7. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: 320-322. A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

The Invention

8. The claimed invention is a method of using bit vector indexes in order to increase the efficiency of database querying.

Claim Objections

9. In view of the amendment to claims 14, 35, 42, 48, 56 and 63, the examiner withdraws all pending claim objections.

10. The examiner advises the Applicants, however, that the amendment to claim 42 does not appear to be what was intended by the Applicants. The Applicants' remarks indicate that the term "affects" would be replaced by "should effect". In claim 42, however, the term "effect" has in fact been replaced by "affect".

11. Claims 2, 23 and 44 are objected to because of the following informalities:

Regarding claims 2, 23 and 44, these claims contain the new limitation "encoded bit representation", while the claims depending from them refer to "encoded bit vector representation". Since the limitations are apparently referring to the same feature, the terms should be consistent.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

13. Claims 1-63 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

14. Claims 1, 22 and 43 are vague, unclear, and/or indefinite. In these claims, the term 'value' is used ambiguously.

In the preamble and steps 1, 2 and 3, the term 'value' refers to the association of a specific data value (e.g., 1, 'Apex', 'Monitor') and a specific data field (e.g., Manufacturer ID, Manufacturer, Category). For example, a 'value' could be 'Manufacturer ACME'.

In the fourth step, however, the term 'value' refers to the '1' or '0' entered in the bit position to represent the presence or absence of the specific data value cited above.

In the fifth step, the value refers to the contents of the field of the data record under consideration.

Furthermore, in the fifth step, the claimed step is that the 'bit position' is synchronized to reflect updates to the value. However, it is the *contents* of the bit position that is synchronized, and it must reflect updates to the *contents of the field of the data record under consideration*, not to the value. The value (as defined in the preamble and in steps 1, 2 and 3) cannot change, since the bit vector itself represents this specific value.

In addition, the amended limitation "associating a bit position of a bit vector representation to the at least one record in a lookup table that contains an association of the value with an identification value utilized to point to the bit pattern" renders the claim indefinite.

The limitation "at least one data record" in the preamble refers to a record in the products table (using the example tables of Figure 3), but in this limitation, "the at least one record" refers to a lookup table. Also, it is unclear to the examiner how the bit position can be associated with a record in a lookup table and still be consistent with the specification. In Figure 3, for instance, each position of the bit vectors is associated with a record in the products table.

Finally, it is unclear what "associating a bit position...with a record in the lookup table...utilized to point to the bit position" means. The records in the lookup tables are merely utilized to decode the meanings of values in the corresponding columns of the products table. The examiner cannot understand how the lookup tables can be utilized to point to the bit positions in the bit vectors.

15. Claims 2-15, 23-36 and 44-57, incorporating the above cited deficiencies, are therefore also rendered indefinite.

16. Regarding claims 16, 37 and 58, the second limitation states that a second bit vector representation is created for a second combination of field values. The limitation continues that the second bit vector identifies "use of a search for the first combination of field values in at least one data record." Even given the relevant portion of the specification on page 23 et seq., the meaning of this limitation is unclear to the examiner. Does the second bit vector represent a second combination of field values, or some representation of the first field values? It is furthermore unclear to the examiner what feature of the second bit vector would cause it to be characterized as a *search* bit vector (as it is in the Applicants' Remarks, page 4, second to last paragraph), when the first bit vector is not.

The Applicants are requested to provide further explanation as to the proper interpretation of this limitation, as well as a citation of the specific embodiment in the specification, including pages and drawing figures, that the claims are intended to reflect.

17. Claims 17-21, 38-42 and 59-63, incorporating the above cited deficiencies, are therefore also rendered indefinite.

18. Regarding claims 19, 40 and 61 it is claimed that performing a logical "AND" will result in a single result representing whether any of the at least one data records contains a combination of the at least first and second values. However, the result of such a logical "AND" operation will represent whether any of the records contain the first value and any of the records contain the second value; the values need not occur in the same record for a logical "AND" to return a '1'.

For example, if record number 1 contains value1, and record number 2 contains value2, a bitwise "AND" operation (01 & 10) will correctly result in a 00, indicating that there are no records that contain both value1 and value2. However, a *logical* "AND" operation (01 && 10) will result in a 1, indicating that both values were non-zero. Note that the values (value1 and value2) need not be in the same record for the operation to return a positive result.

19. Claim 29 recites the limitation "the encoded bit vector" in line 3. There is insufficient antecedent basis for this limitation in the claim.

20. Claims 11, 32 and 53 recite the limitation "the data structure" in line 2. There is insufficient antecedent basis for this limitation in the claim.

21. Claim 56 recites the limitation "the bit-level operation" in line 2. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 103

22. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

23. The factual inquiries set forth in *Graham* v. *John Deere Co*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

24. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

25. Claims 16-18, 37-39 and 58-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes") in view of **Chadha et al.** (U.S. Patent 5,706,495).

26. Regarding claims 16, 37 and 58, **O'Neil et al.** [1] teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values, comprising:

a) creating a first bit vector representation for a first value, the first bit vector representation identifying use of the first value in the at least one data record (see the disclosure of the creation of bitmap indexes in section 2.1.1 Bitmap Indexes, page 39);

b) creating a second bit vector representation for a second value, the second bit vector representation identifying use of the second value in the at least one data record (see the disclosure of the creation of bitmap indexes in section 2.1.1 Bitmap Indexes, page 39); and

c) performing a bit-level operation on the first and second bit vector representations (see disclosure of the database query performance of Boolean operations, including "AND" and "OR" operations, on bitmap indexes, section 2.1.2, pages 39-40).

O'Neil et al. [1] does not explicitly teach a method, computer-readable medium and computer-executable process wherein the bit vector representations are associated with a combination of field values identified by utilizing at least two look-up tables.

Chadha et al., however, teaches a method, computer-readable medium and computer-executable process wherein the bit vector representations are associated with a combination of field values identified by utilizing at least two look-up tables (see col. 3, lines 29-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to associate a bit vector with a combination of field values identified by utilizing at least two look-up tables, since this allows a single index to be maintained for each attribute, and because indices on multiple attributes are not needed (see col. 7, lines 65-67), thus providing the advantage of saving memory space while maintaining all data required to process queries.

27. Regarding claims 17, 18, 38, 39, 59 and 60, **O'Neil et al. [1]** teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values wherein the bit-level operation is a bit-wise "AND" returning a bit corresponding to each of the at least one data record identifying whether a combination of the first and second values exist in the at least one data record (see disclosure of the database query performance of Boolean operations, including "AND" and "OR" operations, on bitmap indexes, section 2.1.2, pages 39-40).

28. Claims 1-4, 11, 12, 22-25, 32, 33, 43-46, 53 and 54 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al. [1]** ("Improved Query Performance with Variant Indexes") in view of **Chadha et al.** (U.S. Patent 5,706,495) in view of **Depledge et al.** (U.S. Patent 5,884,307).

29. Regarding claims 1, 22 and 43, **O'Neil et al. [1]** teaches a method, computer-readable medium and computer-executable process for indexing occurrences of a value in at least one data record using a bit vector representation, comprising:

a) associating a bit vector representation with a value (see section 2.1.1 Bitmap Indexes, page 39; the claimed value is anticipated by property P in the second paragraph of col. 2);

b) associating a bit position of the bit vector representation to the at least one record (see section 2.1.1 Bitmap Indexes, page 39, specifically col. 2, second paragraph, lines 1-4);

c) determining whether the value exists in the at least one data record (see section 2.1.1 Bitmap Indexes, page 39, specifically col. 2, second paragraph, lines 1-4); and

d) assigning a binary value to the bit position in the bit vector representation based on the outcome of the determining step (see section 2.1.1 Bitmap Indexes, page 39, specifically col. 2, second paragraph, lines 1-4).

O'Neil et al. [1] does not explicitly teach a method, computer-readable medium and computer-executable process wherein the bit vector representation is associated with a plurality of values encountered in at least two data fields.

Chadha et al., however, teaches a method, computer-readable medium and computer-executable process wherein the bit vector representation is associated with a plurality of values encountered in at least two data fields (see col. 3, lines 29-35).

It would have been obvious to one of ordinary skill in the art at the time of the invention to associate a bit vector with a plurality of values encountered in at least two data fields, since this

allows a single index to be maintained for each attribute, and because indices on multiple attributes are not needed (see col. 7, lines 65-67), thus providing the advantage of saving memory space while maintaining all data required to process queries.

Neither **O'Neil et al. [1]** nor **Chadha et al.** explicitly teaches a method, computer-readable medium and computer-executable process including the step of synchronizing the bit position with the value to reflect any updates to the value.

Depledge et al., however, teaches a method for updating a segmented bitmapped index (analogous to the claimed bit vector index) to reflect a change made to data upon which the segmented index is based (see Abstract; see also col. 2, line 65 through col. 3, line 32).

It would have been obvious to one of ordinary skill in the art to provide for the synchronization of the claimed bit vector with the data upon which the index is based, since for the bitmapped indexes to remain valid, they must be updated whenever a change is made to the data upon which they are based (see col. 2, lines 25-37).

30. Regarding claims 2-4, 23-25 and 44-46, **O'Neil et al. [1]** additionally teaches a method, computer-readable medium and computer-executable process substantially as claimed, including the fact that the bit vector representation comprises a sequence of bits (see **O'Neil et al. [1]** page 39, col. 2, first sentence of the second paragraph), further comprising encoding the bit vector representation by determining whether a frequency of a binary digit is less than the number of bits used to store a number, and storing as the encoded bit vector representation at least one position of

the binary digit in the bit vector representation (see disclosure that when the disk space required to hold a bitmap column index is comparable to the disk space required for the RID-list index, the representation is changed from a bitmap to a RID list, a rowed being analogous to the claimed position of the bit, page 39, last paragraph of section 2.1.1 Bitmap Indexes).

31. Regarding claims 11, 32 and 53, **O'Neil et al. [1]** additionally teaches a method, computer-readable medium and computer-executable process wherein the data structure is a record in a database (see disclosure of bitmap creation for 'the n rows of a table T', analogous to the claimed records in a database, page 39, col. 1, last paragraph).

32. Regarding claims 12, 33 and 54, **O'Neil et al. [1]** additionally teaches a method, computer-readable medium and computer-executable process further comprising examining the bit vector representation to determine whether the data record contains the value (see discussion of the bitmap index performance in section 2.1.2, pages 39-40).

33. Claims 5-10, 13-15, 26-31, 34-36, 47-52 and 55-57 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al. [1]** ("Improved Query Performance with Variant Indexes") in view of **Chadha et al.** (U.S. Patent 5,706,495) in view of **Depledge et al.** (U.S. Patent 5,884,307) as applied to claims 1, 22 and 43 above, and further in view of **O'Neil et al. [2]** ("Multi-Table Joins Through Bitmapped Join Indices").

34. Regarding claims 5-7, 26-28 and 47-49, **O'Neil et al. [1], Chadha et al.** and **Depledge et al.** teach a method, computer-readable medium and computer-executable process substantially as claimed, including the fact that the bit vector representation comprises a sequence of bits (see **O'Neil et al. [1]** page 39, col. 2, first sentence of the second paragraph).

None of **O'Neil et al. [1], Chadha et al.** nor **Depledge et al.** explicitly teaches a method, computer-readable medium and computer-executable process further comprising encoding the bit vector representation by determining whether the size of a region of like binary digits is twice number of bits used to store a number, and storing as the encoded bit vector representation a representation of the region.

O'Neil et al. [2], however, teaches a method, computer-readable medium and computer-executable process further comprising encoding the bit vector representation by determining whether the size of a region of like binary digits is twice number of bits used to store a number, and storing as the encoded bit vector representation a representation of the region (see the disclosure regarding run-length encoding, page 9, last sentence of the last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the manner of storage as claimed, since this would save in data storage, as disclosed in the last paragraph of page 9.

35. Regarding claims 8-10, 29-31 and 50-52, **O'Neil et al. [1], Chadha et al.** and **Depledge et al.** teach a method, computer-readable medium and computer-executable process substantially as claimed.

None of **O'Neil et al. [1], Chadha et al.** nor **Depledge et al.** explicitly teaches a method, computer-readable medium and computer-executable process wherein the bit vector representation is encoded and compressed using a compression technique.

O'Neil et al. [2], however, teaches a method, computer-readable medium and computer-executable process wherein the bit vector representation is encoded and compressed using a compression technique (see the disclosure regarding bitmap compression, including run-length encoding, page 9, bottom of the last paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to change the manner of storage as claimed, since this would save in data storage, as disclosed in the last paragraph of page 9.

36. Regarding claims 13-15, 34-36 and 55-57, **O'Neil et al. [1]** additionally teaches a method, computer-readable medium and computer-executable process wherein plural bit vector representations exist each representing a discrete value, and further comprising determining whether the data record contains more than one of the values by performing a bit-level operation that includes "OR" and "AND" on the corresponding bit vector representations (see disclosure of the

database query performance of Boolean operations, including "AND" and "OR" operations, on bitmap indexes, section 2.1.2, pages 39-40).

37. Claims 19, 40 and 61 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al. [1]** ("Improved Query Performance with Variant Indexes") in view of **Chadha et al.** (U.S. Patent 5,706,495) as applied to claims 16-18, 37-39 and 58-60 above, and further in view of **Schildt** ("C: The Complete Reference").

38. Regarding claims 19, 40 and 61, **O'Neil et al. [1]** and **Chadha et al.** teach a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values substantially as claimed.

Neither **O'Neil et al. [1]** nor **Chadha et al.** explicitly teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record wherein the "AND" operation is a logical "AND" returning a single result representing whether any of the at least one data records contain a combination of the first and second values.

Schildt, however, teaches the use of the logical "AND" operator to determine whether or not all of the expressions are non-zero (see pages 47-49).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use the logical "AND" operator, since this would allow a user to determine whether or not the first and second bit vector representations were both non-zero.

39. Claims 20, 21, 41, 42, 62 and 63 are rejected under 35 U.S.C. 103(a) as being unpatentable over **O'Neil et al.** [1] ("Improved Query Performance with Variant Indexes") in view of **Chadha et al.** (U.S. Patent 5,706,495) as applied to claims 16-18, 37-39 and 58-60 above, and further in view of **Depledge et al.** (U.S. Patent 5,884,307).

40. Regarding claims 20, 21, 41, 42, 62 and 63, **O'Neil et al.** [1] and **Chadha et al.** teach a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values substantially as claimed.

Neither **O'Neil et al.** [1] nor **Chadha et al.** explicitly teaches a method, computer-readable medium and computer-executable process for identifying combinations of values used in at least one data record comprising fields for storing the values further comprising updating at least one data record, determining whether the updating has affected any of the bit vector representations, and if so, updating the affected bit vector representations.

Depledge et al., however, teaches a method for updating a segmented bitmapped index (analogous to the claimed bit vector index) to reflect a change made to data upon which the segmented index is based (see Abstract; see also col. 2, line 65 through col. 3, line 32).

It would have been obvious to one of ordinary skill in the art to provide for the synchronization of the claimed bit vector with the data upon which the index is based, since for the bitmapped indexes to remain valid, they must be updated whenever a change is made to the data upon which they are based (see col. 2, lines 25-37).

Response to Arguments

41. Applicant's arguments filed 17 July 2003 have been fully considered but they are not persuasive.

42. Regarding the Applicants' argument that the rejection of claims 1, 22 and 43 under 35 U.S.C. § 112, because of the use of the "synchronization of the bit position" language is erroneous, the examiner responds that the cited "rank" value does not appear in the claims, and neither can the examiner locate any mention of such a value in the specification. It is unclear how the existence of a "rank" value renders the claim language proper, or for that matter what the "rank" value does.

43. Regarding the Applicants' arguments that the rejection of claims 19, 40 and 61 under 35 U.S.C. § 112 is erroneous, the examiner responds that the Applicants fail to explain how the "rank"

value will cause the execution of a logical AND operation to operate differently in the context of the instant invention than in a conventional computer system.

Furthermore, the cited "rank" value does not appear in the claims, and neither can the examiner locate any mention of such a value in the specification.

44. The Applicants are reminded that they have yet to respond to the rejection of claims 11, 32 and 53 under 35 U.S.C. § 112. Any response that fails to address this rejection will be held non-responsive.

45. Regarding the Applicants' arguments concerning claims 16, 37 and 58, these arguments have not been addressed in view of the claim rejections based on 35 U.S.C.§ 112, due to the new language introduced by the amendment.

Furthermore, on page 5, top paragraph of the Applicants' Remarks, the argument is made that the reference fails to teach various features, such as "using the numerical value's value (or content) as a pointer in a bit array" and "utilizing lookup tables to order (e.g. sort or rank) values from a specific field in a database table". However, these are not limitations that appear in the claims, and so these arguments are rendered moot.

46. Like the Applicants' arguments concerning claims 16, 37 and 58, the remarks concerning claims 1, 22 and 43 include arguments that the prior art fails to teach features that are not cited in these claims, such as "consult[ing] the lookup table to build a search bit string". Since these limitations are not claimed, these arguments are rendered moot.

Conclusion

47. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Luke S. Wassum whose telephone number is 703-305-5706. The examiner can normally be reached on Monday-Friday 8:30-5:30, alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John E. Breene can be reached on 703-305-9790. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

In addition, INFORMAL or DRAFT communications may be faxed directly to the examiner at 703-746-5658.

Customer Service for Tech Center 2100 can be reached during regular business hours at (703) 306-5631, or fax (703) 746-7240.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

Luke S. Wassum
Art Unit 2177

lsw
27 October 2003

JOHN BREENE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100